## In the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1.-24. (Canceled)

25. (Currently Amended) A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion programmed for reading in a computational instruction;

a decoding portion programmed for decoding the computational instruction that has been read in;

an execution portion programmed for executing the computational instruction in accordance with a decoding of the computational instruction;

a sequencer programmed for updating an output to one of at least three different states as a conditional execution status in response to an instruction decoding operation among the computational instruction and subsequent instructions including a plurality of instructions that are sequentially arranged as an instruction sequence after the computational instruction; and

an instruction overriding control circuit programmed for controlling an overriding of any instruction of the subsequent instructions ~~that follow the computational instruction~~ in response to ~~a~~ the conditional execution status updated by ~~a~~ the sequencer ~~in accordance with the decoding of the computational instruction~~.

26. (Currently Amended) The data processing device according to claim 25, wherein the instruction overriding control circuit overrides none of the subsequent instructions in response to a value of a status flag determined by execution of the computational instruction regardless of the conditional execution status updated by the sequencer.

27. (Currently Amended) A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion programmed for reading in a computational instruction;

a decoding portion programmed for decoding the computational instruction that has been read in;

an execution portion programmed for executing the computational instruction in accordance with a decoding of the computational instruction;

a sequencer programmed for updating an output to one of at least three different states as a conditional execution status in response to an instruction decoding operation among the computational instruction and subsequent instructions including a plurality of instructions that are sequentially arranged as an instruction sequence after the computational instruction; and

an instruction overriding control circuit programmed for overriding at least one instruction of the subsequent instructions, ~~that follow the computational instruction~~ the at least one instruction designated in response to a value of a status flag determined by execution of the computational instruction and the conditional execution status updated by ~~a~~ the sequencer ~~in accordance with the decoding of the computational instruction~~.

28. (Previously Presented) The data processing device according to claim 27, wherein the instruction overriding control circuit overrides the at least one instruction by overriding an execution of the at least one instruction in the execution portion.

29. (Canceled)

30. (Currently Amended) The data processing device according to claim 27, wherein the subsequent instructions include a first instruction and a second instruction, and the computational instruction, ~~and a~~ the first instruction, and ~~a~~ the second instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides ~~either~~ one of the first instruction ~~or~~ and the second instruction ~~in response to the conditional execution status updated by the sequencer~~ when the status flag takes a given value.

31. (Currently Amended) The data processing device according to claim 30, wherein the instruction overriding control circuit overrides ~~either~~ another one of the first instruction ~~or~~ and

the second instruction ~~in accordance with the conditional execution status and a status flag determined by execution of the computational instruction~~ when the status flag takes a different value from the given value.

32. (Currently Amended) The data processing device according to claim 30, wherein ~~neither~~ each of the first instruction ~~nor~~ and the second instruction ~~includes~~ does not have any condition ~~to be overridden~~ for indicating an overriding of any instruction arranged after the computational instruction,

wherein the subsequent instructions are not any branch instructions.

33. (Currently Amended) The data processing device according to claim [[30]] 27, wherein the subsequent instructions include a first instruction group including a plurality of instructions and a second instruction group including a plurality of instructions, and the computational instruction, ~~and a~~ the first instruction group, ~~including a plurality of instruction strings~~ and ~~a~~ the second instructional group ~~including a plurality of instructional strings~~ are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides ~~either~~ one of the first instruction group ~~or~~ and the second instruction group ~~in response to the conditional execution status updated by the sequencer~~ when the status flag takes a given value.

34. (Currently Amended) The data processing device according to claim 33, wherein the instruction overriding control circuit overrides ~~either~~ another one of the first instruction group ~~or~~ and the second instruction group ~~in accordance with the conditional execution status and a status flag determined by execution of the computational instruction~~ when the status flag takes a different value from the given value.

35. (Currently Amended) The data processing device according to claim 33, wherein ~~no instructions~~ any instruction included in both the first instruction group and the second instruction group ~~include~~ does not have any ~~conditions to be overridden~~ condition for indicating an overriding of any instruction arranged after the computational instruction,

wherein the subsequent instructions are not any branch instructions.

36. (Currently Amended) The data processing device according to claim 27, wherein the subsequent instructions include a first instruction and a second instruction, and the computational instruction, ~~and a~~ the first instruction, and the second instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides only the first instruction ~~in response to the conditional execution status updated by the sequencer~~ only when the status flag takes a given value.

37. (Canceled)

38. (Currently Amended) The data processing device according to claim 36, wherein the first instruction does not ~~include~~ have any condition ~~to be overridden~~ for indicating an overriding of any instruction arranged after the computational instruction,

wherein the subsequent instructions are not any branch instructions.

39. (Currently Amended) The data processing device according to claim 27, wherein the subsequent instructions include a first instruction group including a plurality of instructions and a second instruction group including a plurality of instructions, and the computational instruction, ~~and a~~ the first instruction group, and the second instruction group ~~including a plurality of instruction strings~~ are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides only the first instruction group ~~in response to the conditional execution status updated by the sequencer~~ only when the status flag takes a given value.

40. (Canceled)

41. (Currently Amended) The data processing device according to claim 39, wherein ~~no instructions~~ any instruction in the first instruction group ~~include~~ does not have any ~~conditions to be overridden~~ condition for indicating an overriding of any instruction arranged after the computational instruction,

wherein the subsequent instructions are not any branch instructions.

42. (Currently Amended) A data processing device reading in and executing instructions in a certain sequence, the data processing device comprising:

a fetch portion programmed for reading in a computational instruction;

a decoding portion programmed for decoding the computational instruction that has been read in;

an execution portion programmed for executing the computational instruction in accordance with a decoding of the computational instruction;

a sequencer programmed for updating an output to one of at least three different states as a conditional execution status in response to an instruction decoding operation among the computational instruction and subsequent instructions including a plurality of instructions that are sequentially arranged as an instruction sequence after the computational instruction; and

an instruction overriding control circuit programmed for overriding at least one instruction of the subsequent instructions, ~~that follow the computational instruction~~ the at least one instruction designated in response to a value of a status flag determined by execution of the computational instruction and the conditional execution status updated by a the sequencer ~~in accordance with the decoding of the computational instruction, wherein the instruction overriding control circuit overrides the at least one instruction~~ by allowing the fetch portion to skip reading in the at least one instruction.

43. (Previously Presented) The data processing device according to claim 42, wherein the fetch portion includes a plurality of buffers to override the at least one instruction.

44. (Currently Amended) The data processing device according to claim 42, wherein the subsequent instructions include a first instruction and a second instruction, and the computational instruction, ~~and a~~ the first instruction, and a the second instruction are sequentially arranged as an instruction sequence,

wherein the overriding control circuit overrides ~~either an execution~~ one of the first instruction ~~in the execution portion or reading in of~~ and the second instruction ~~in the fetch portion in accordance with the conditional execution status and a status flag determined by~~

~~execution of the computational instruction~~ by allowing the fetch portion to skip reading in the one of the first instruction and the second instruction when the status flag takes a given value.

45. (New) The data processing device according to claim 44, wherein the instruction overriding control circuit overrides another one of the first instruction and the second instruction by overriding an execution of the another one of the first instruction and the second instruction in the execution portion when the status flag takes a different value from the given value.